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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,488	08/30/2000	Donald C. Englin	RA 5265 (33012/294/101)	9980

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	11

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,488	ENGLIN ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 29, 2003 has been entered.

Claim Objections

2. Claim 2 is objected to because of the following informalities:

In claim 2, line 2, after "tag memory", it appears that "responsive" should be changed to –responsively--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6, 10-12, 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Freerksen et al (US6,314,491).

As per claims 1 and 6, Freerksen discloses a data processing system having a processor responsively coupled to a store-in cache memory which is responsively coupled to a lower level memory [*processors 24a, 24b coupled to L1 caches 28a, 28b and to L2 cache 26 and main storage 14*; Fig.2; *L1 cache is a write back cache (also known as a store-in cache in the art)*; col. 6, line 64 – col. 7, line 4], the improvement comprising a flush buffer directly coupled to said store-in cache memory and said lower level memory [*intermediate cache buffer 30 is directly coupled to L1 caches 28a, 28b; to L2 cache 26 and main storage 14*; Fig. 2; *data is cast back into cache buffer 30 which is an intermediate storage area*; col. 6, lines 41 – col. 7, line 4].

As per claim 2, Freerksen discloses a tag memory responsively coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor [*line 52 comprises a tag field which identifies the address of the data and state field identifies the state of the line*; col. 7, lines 32-43].

As per claims 3 and 10, Freerksen discloses a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by the processor [*logic in storage control unit 22 manages the process of obtaining and delivering to/from cache buffer 30*; col. 7, lines 1-13; *a flush write back command is generated when there is a modified version in the line in the L1 cache*; col. 8, line 61 – col. 9, line 11].

As per claim 11, Freerksen discloses a method of flushing a store-in cache memory comprising:

a. receiving a data request at said store-in cache memory [*processor 24 interacts with L1 cache to obtain and store needed data*; col. 5, lines 26-28; *L1 cache is a write back cache (also known as a store-in cache in the art)*; col. 6, line 64 – col. 7, line 4];

b. searching said store-in cache memory in response to said data request [*directory identifies memory location for which copies currently reside in*; col. 5, lines 41-46];

c. experiencing a cache miss in response to said searching step [*L1 cache is not storing the requested data*; col. 5, lines 53-59];

e. selecting a particular location within said store-in cache memory to be flushed buffer [*when there is a miss in L1 cache, a line in cache buffer 30 is assigned to the miss*; col. 6, lines 58 – col. 7, line 4]; transferring data from said particular location to a flush buffer [*when there is a miss in L1 cache, a line in cache buffer 30 is assigned to the miss, the data is stored in the assigned line of cache buffer 30*; col. 6, lines 58-64].

As per claim 12, Freerksen discloses determining whether a particular location was modified by a processor [*the located cache line (CL) is evaluated to determine whether it is marked "modified"*; col. 7, lines 64 – col. 8, line 4].

As per claim 16, Freerksen discloses an apparatus comprising:

a. means for executing program instructions [*processors 24a, 24b*; Fig.2];

b. means responsively coupled to said executing means for caching data on a store-in basis [*L1 caches 28a, 28b*; Fig.2; *L1 cache is a write back cache (also known as a store-in cache in the art)*; col. 6, line 64 – col. 7, line 4];

c. Means directly coupled to said caching means for buffering data from said caching means to be flushed [*intermediate cache buffer 30 is directly coupled to L1 caches 28a, 28b*; Fig. 2; *data is cast back into cache buffer 30 which is an intermediate storage area*; col. 6, lines 41 – col. 7, line 4].

As per claim 17, Feerksen discloses means responsively coupled to said caching means for selecting said data to be flushed [*logic in storage control unit 22 manages the process of obtaining and delivering to/from cache buffer 30*; col. 7, lines 1-13].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Jeddeloh (US6,460,114).

As per claim 13, Freerksen discloses the claimed invention as detailed above in the previous paragraphs. However, Freerksen does not specifically teach inhibiting said transferring step if said determining step determines that said data within said particular location was not modified by said processor as recited in the claim.

Jeddeloh discloses inhibiting a transferring step if a determining step determines that the data within a particular location was not modified by a processor [*clean data not transferred to temporary buffer*; col. 2, lines 5-10].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Jeddeloh before him at the time the invention was made, to modify the system of Freerksen to include inhibiting a transferring step if a determining step determines that the data within a particular location was not modified by a processor because it would have reduced the memory latency time experienced by the CPU by selecting an existing cache line for replacement based on a status indication [col. 2, lines 1-24] as taught by Jeddeloh.

7. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Jeddeloh (US6,460,114) and Kurosawa (US6,418,515).

As per claim 14, the combination of Freerksen and Jeddeloh discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Freerksen and Jeddeloh does not specifically teach routing said data from said particular location to an available one of said first flush store and said second buffer store as recited in the claim.

Kurosawa discloses routing data from a particular location to an available one of a first flush buffer store and a second buffer store [*data is registered in the write-back buffer 403 at the second stage when write-back buffer 402 becomes free*; col. 29, lines 11-58; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Kurosawa before him at the time the invention was made, to modify the system of Freerksen to include routing data from a particular location to an available one of a first flush buffer store and said second buffer store because it would have it would have provided a cache flush unit which implement a quick cache flush and reduce overhead in checkpoint processing by allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

As per claim 15, Freerksen discloses rewriting said data to a lower level memory following said transferring step [*data in cache buffer is transferred to L2 cache or main memory*; col. 7, lines 1-4].

8. Claims 4-5, 7-9 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Kurosawa (US6,418,515).

As per claims 4, 7 and 18, Freerksen discloses the claimed invention as detailed above in the previous paragraphs. However, Freerksen does not specifically teach a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output as recited in the claims.

Kurosawa discloses a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output [*cache flush unit comprises write-back buffer 401 and write-back buffer 403 for cache flush*; col. 26, lines 31-40; *each write-back buffer has an input and an output*; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Kurosawa before him at the time the invention was made, to modify the system of Freerksen to include a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output because it would have provided a cache flush unit which implement a quick cache flush and reduce overhead in checkpoint processing by

allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

As per claims 5, 8 and 19, Freerksen discloses the claimed invention as detailed above in the previous paragraphs. However, Freerksen does not specifically teach a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer store as recited in the claims.

Kurosawa discloses a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer [*prefetching buffer 322 coupled to write-back buffers 401-403, data is registered in the write-back buffer 403 at the second stage when write-back buffer 402 becomes free*; col. 29, lines 11-58; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Kurosawa before him at the time the invention was made, to modify the system of Freerksen to include a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer because it would have shortened the searching time associated with cache flush by checking the value of a bit to determine whether the data is received by the prefetching buffer [col. 30, lines 8-10] and provided a cache flush unit which

implement a quick cache flush and reduce overhead in checkpoint processing by allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

As per claim 9, Freerksen discloses a tag memory responsively coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor [*cache line 52 comprises a tag field which identifies the address of the data and state field identifies the state of the line*; col. 7, lines 32-43].

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Kurosawa (US6,418,515) and Jeddeloh (US6,460,114).

As per claim 20, the combination of Freerksen and Kurosawa discloses the claimed invention as detailed above in the previous paragraphs.

Freerksen further discloses means responsively coupled to said caching means for determining whether data has been modified by said executing means [*cache line 52 comprises a tag field which identifies the address of the data and state field identifies the state of the line*; col. 7, lines 32-43].

However, the combination of Freerksen and Kurosawa does not specifically teach means responsively coupled to said determining means and said buffering means for inhibiting transfer of data from said caching means to said buffering means if said

determining means determines that said data has not been modified by said executing means as recited in the claim.

Jeddeloh discloses means responsively coupled to a determining means and a buffering means for inhibiting transfer of data from a caching means to a buffering means if said determining means determines that said data has not been modified by an executing means [*clean data not transferred to temporary buffer*; col. 2, lines 5-10].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Jeddeloh before him at the time the invention was made, to modify the system of Freerksen to include means responsively coupled to a determining means and a buffering means for inhibiting transfer of data from a caching means to a buffering means if said determining means determines that said data has not been modified by an executing means because it would have reduced the memory latency time experienced by the CPU by selecting an existing cache line for replacement based on a status indication [col. 2, lines 1-24] as taught by Jeddeloh.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach second level cache flushing, flush buffer and cache line modification.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Pierre M. Vital
Art Unit 2188
November 6, 2003